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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,048	12/06/2001	Yasurou Matsuzaki	108397-00052	4931

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	10/003,048	MATSUZAKI, YASUROU	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE f this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,18,19,21,22,35 and 36* is/are rejected.

7)☒ Claim(s) *8-16 and 23-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 35 and 36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 35 and 36, it is not clear of "to predetermined delay time" and "to the transition edge of a standard time signal" in lines 7 and 11, respectively. Please clarify the relationship of "to predetermined delay time" in claim 35. The same applied to claim 36.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 18, and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Collins et al. (U. S. PAT. 6,031,847).

In claims 1-6, Collins et al. teaches all claimed features in Figs.3-5, an input/output interface, wherein a logical value (data value) is expressed by an order that transition edges (positive/leading or negative/trailing edges) appear in a plurality of transmission signals (data signals inside 501) transmitting respectively on a plurality of

signal lines (310-313); wherein each of said transmission signals include a plurality of the transition edges (plurality of positive edges or plurality of negative edges, not shown); and said logical value is expressed by combining the order that the respective transition edges appear in the transmission signals; wherein: said transmission signals (the data signals inside 501) are pulse signals; and said logical value is expressed by using the order that the transition edges appear in the pulse signals; wherein said logical value is expressed by combining the order that leading edges appear in and the order that trailing edges appear in said pulse signals; wherein said plurality of the signal lines (310-313) consists of three lines or more (4 lines); and wherein said transmission signals express one (data) or both of data and an address.

In claim 18, Collins et al. teaches all claimed features in Fig. 3-5, the input/output interface according to claim 1, wherein a transmitting circuit (301) for transmitting said transmission signals (Channel 0-3) and a receiving circuit (302) for receiving said transmission signals are respectively formed on separate semiconductor chips (col. 1, line 9; between digital systems, read as two separate chips).

In claim 35, Collins et al. teaches all claimed features in Figs. 3-5, a semiconductor integrated circuit comprising: a transmitting circuit (301) for converting a logical value (data vaue), expressed with a plurality of bits (word bits), to predetermined delay time (skew), and for outputting a transmission signal, which is behind a standard timing signal (clock not shown) by the delay time, to a signal line (313).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Cecchi et al. (U. S. PAT. 6,304,106).

In claim 21, Cecchi et al. teaches all claimed features in Fig. 2, a semiconductor integrated circuit comprising a receiving circuit (Fig. 2), including: a comparing circuit (102) for comparing an order that transition edges (A, B, C) appear in a plurality of transmission signals transmitting respectively through a plurality of signal lines (input lines to 102); and a logical value generating circuit (106) for generating a logical value (Z) according to a result of the comparison by said comparing circuit.

5. Claims 1, 7, 22, and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Jeong (U. S. PAT. 5,712,884).

In claims 1 and 7, Jeong teaches all claimed features in Figs. 1 and 6, an input/output interface, wherein a logical value (INPUT DATA) is expressed by an order that transition edges (positive/leading or negative/trailing edges) appear in a plurality of

transmission signals (Q0-Q9) transmitting respectively on a plurality of signal lines (signal lines that carry Q0-Q9); wherein the input/output interface having a transmitting device (Fig. 1) for transmitting said transmission signals, the device comprising: a transmitting circuit (14) for selecting any of a plurality of timing signals (CK0-CK9) for each of said signal lines according to said logical value, the plurality of timing signals at transition edges having timings different from each other (Timing graph of Fig. 6), and for generating each of said transmission signals in synchronization with each of the selected timing signals, respectively.

In claim 22, Jeong teaches all claimed features in Figs. 1 and 6, an input/output interface, wherein a logical value (input data) is expressed by a time difference between a transition edge of a transmission signal (Q0) transmitting on a signal line and a transition edge of a standard timing signal (CK0).

In claim 36, Jeong teaches all claimed features in Figs. 1 and 6, a semiconductor integrated circuit comprising: a receiving circuit (Fig. 1) for detecting a delay time (22) of a transition edge of a transmission signal transmitting through a signal line (input data), to the transition edge of a standard timing signal (input clock), and for generating a logical value (Q0) according to the detected delay time.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Collins et al.

In claim 19, Collins et al. teaches all claimed features in Fig. 3-5, the input/output interface according to claim 1, wherein a transmitting circuit (301) for transmitting said transmission signals (Channel 0-3) and a receiving circuit (302) for receiving said transmission signals; with the exception of showing that the transmitter circuit and the receiver circuit are both formed on the same semiconductor.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to integrate the transmitter circuit and the receiver circuit, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. Howard v. Detroit Stove Works, 150 U.S. 164 (1893).

8. Claims 8-16 and 23-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claim 20 is allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (703) 306-5948. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (703) 305-3493. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-6251 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0959.

Vibol Tan

Patent Examiner, AU 2819